

REMARKS/ARGUMENTS

Claims 1-4 and 6-18 are pending in the present application. Claims 1-4 and 6 are amended. Claims 7-18 are new. Claims 1, 6 and 10 are independent claims. The Examiner is respectfully requested to reconsider his rejections in view of the Amendments and Remarks as set forth hereinbelow.

Claim Objections

In the Office Action, the Examiner objected to claims 3 and 4 because "a control circuit" in lines 5-6 of claim 3 should be changed to "said control circuit." Applicant respectfully submits that claim 3 has been amended above to correct this informality. Accordingly, withdrawal of this objection is respectfully requested.

Rejection Under 35 U.S.C. § 112

Claims 4 stands rejected under 35 USC § 112, second paragraph, because of the "said output circuit" in line 3 of claim 4 lacks antecedent basis. Applicant respectfully submits claim 4 has been amended such that each recited feature now contains sufficient antecedent basis. Thus, withdrawal of this rejection is respectfully requested.

Rejection Under 35 U.S.C. § 103

Claims 1 and 6 stand rejected under 35 USC § 103(a) as being unpatentable over Japanese patent document 2000-020459 to Nakajima et al. (hereinafter "Nakajima") in view of U.S. Patent No. 6,134,621 to Kelley et al. (hereinafter "Kelley") and U.S. Patent No. 5,481,679 to Higaki et al. (hereinafter "Higaki"). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

As amended, independent claims 1 and 6 recite controlling each of a plurality of switch circuits to turn off the bus connection between a high-speed access device and each of two or more lower-speed access devices when data is transferred to the high-speed access device, and to turn on the bus connection between the high-speed access devices and at least one of the lower-access speed devices when data is transferred to at least one of the lower-speed access devices. Applicant respectfully submits that these features are not taught nor suggested by the combination of Nakajima, Kelley and Higaki.

Specifically, Nakajima and Kelley each discloses that one switch is provided on a data bus in order to enable and disable the bus connection between various devices. As disclosed in Nakajima, a bus switch 5 controls the electrical connection/disconnection of the devices (e.g. 3b) in usual

access field 3 with respect to the data bus 4 and CPU 1. In Kelley, a single switch 123 is provided between PCI slots 117 and 119 (configured for either 66 or 33 MHz and slots 127 and 129 configured for 33 MHz).

Accordingly, neither Nakajima nor Kelley teach or suggest a plurality of switch circuits to turn on and off a bus connection between a device for high-speed access and multiple devices for lower-speed access, as required by independent claims 1 and 6. Applicant further respectfully submits that Higaki fails to provide any disclosure that remedies this deficiency.

Applicant respectfully submits that the amendments to claims 1 and 6, particularly the recitation of multiple switch for turning on and off a bus connection between devices is supported by the originally filed application at, *inter alia*, Fig. 1 and page 7, lines 6-23, of the specification. Accordingly, Applicant submits that these amendments to not add any new matter to the present application.

Applicant respectfully submits that claims 1 and 6 are allowable for at least for the reasons set for the above. Thus, reconsideration and withdrawal of this rejection is respectfully requested.

Claim 2 stands rejected under 35 USC § 103(a) as being unpatentable over Nakajima and Kelley, and further in view of

U.S. Patent No. 6,061,754 to Cepulis et al (hereinafter "Cepulis"). This rejection is traversed.

Cepulis discloses two embodiments. In the first, a computer system 100 has two PCI buses, one being configured for a 33 MHz operating frequency and the other being configured for 66 MHz. Cepulis further discloses that a series of devices ("agents," 441-446) and switches (451-454) may be connected between these two PCI buses, as shown in Fig. 4. According to this first embodiment of Cepulis, the switches determine to which of the PCI buses each agent is connected.

In the second embodiment of Cepulis, as illustrated in Fig. 8, there is one PCI bus to which a series of agents 841-846 and switches 851-854 are connected. Cepulis discloses that in second embodiment, the state of the switches may be set so that either the bus is connected to only two of the agents, or more than two. In this embodiment, Cepulis discloses that the PCI bus operates at a frequency of 66 MHz if only two agents are connected, and 33 MHz if more than two agents are connected.

Each of independent claims 1 and 6 recites that the switch circuits are controlled to turn off the bus connection between the high-speed access device and each of the lower-speed access devices when data is transferred to the high-speed access device, and turn on the bus connection when data is transferred

to at least one of the lower-speed access devices. Applicant respectfully submits that Cepulis fails to disclose these features, and therefore fails to remedy the deficiencies of Nakajima, Kelley and Higaki set forth above in connection with claims 1 and 6.

Specifically, there is no disclosure in Cepulis that any switch is controlled based on which particular device is subject to data transfer. In fact, in the second embodiment utilizing one bus, Cepulis discloses that the user elects which bus agents are connected to the bus via the switches (See Cepulis at column 8: lines 21-25).

Furthermore, Cepulis provides no disclosure that the agents connected by the switches are configured for different access speeds. Instead, Cepulis discloses that the operating speed of each agent is dependent upon the operating frequency of the PCI bus to which it is connected. Thus, in Cepulis, the switches control the access speeds of the devices (by enabling the bus connections), rather than the access speed of the device for data transfer determining how the switches are controlled, as required by claims 1 and 6.

At least for the reasons set forth above, Cepulis fails to remedy the deficiencies of Nakajima, Kelley and Higaki in connection with independent claim 1. Therefore, Applicant

submits that claim 2 is allowable at least by virtue of its dependency on claim 1. The Examiner is, therefore, respectfully requested to reconsider and withdraw this rejection.

Claims 3 and 4 stand rejected under 35 USC § 103(a) as being unpatentable over Nakajima and Kelley, and further in view of U.S. Patent No. 3,594,656 to Tsukamoto (hereinafter "Tsukamoto"). Applicant respectfully submits that Tsukamoto fails to remedy the deficiencies set forth above in connection with independent claim 1. Accordingly, Applicant respectfully submits that claims 3 and 4 are allowable at least by virtue of their dependency on claim 1. It is respectfully requested that the Examiner reconsider and withdraw this rejection.

New Claims

Applicant respectfully submits that new claims 7-9 are allowable at least by virtue of their dependency on allowable claim 6.

It is further respectfully submitted that new independent claim 10 recites a plurality of switches, each of which is configured to disable the bus connection between a corresponding lower-speed access device and the processor when a data transfer is performed with a higher-speed access device. For the reasons set forth above, Applicant respectfully submits that the cited

prior art documents fail to teach or suggest these features, either taken separately or in combination with one another.

Applicant further submits that claims 11-18 are allowable at least by virtue of their dependency on allowable claim 10.

Conclusion

Entry of this Amendment After Final is respectfully requested. In view of the above amendments and remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. Thus, the Examiner is respectfully requested to reconsider and withdraw the various rejections, and issue a Notice of Allowance in connection with the pending claims.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Jason W. Rhodes (Reg. No. 47,305) at the telephone number of (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By



Michael R. Cammarata #39,491

P.O. Box 747

Falls Church, VA 22040-0747

(703) 205-8000

9R
MRC/JWR/mlr/lab